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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,782	03/08/2001	James K. Pickett	5500-64300	8339

7590 03/22/2004

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EXAMINER
CHUNG, CHI WHAN

ART UNIT	PAPER NUMBER
2115	5

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,782	PICKETT, JAMES K.	
	Examiner	Art Unit	
	Chi Whan Chung	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 7, 10 - 18, 21 - 23* is/are rejected.

7)☒ Claim(s) *8 - 9, 19 - 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2, and 4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 12 is objected to because of the following informalities: It is not clear whether claim 12 is dependent on claim 1 or claim 10. Judging from the fact that claims 11, 13 – 15, and 17 all depend on claim 10, the examiner regarded claim 12 as dependent on claim 10. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims1 – 2, 4, 10 – 11, 13, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Loper et al., patent no. 5,805,907.

4. As per claim 1, **Loper et al.** teach a microprocessor comprising:

a plurality of execution units each configured to execute instructions (see units 26, 22, 30, and 36 in Fig. 1);

an instruction dispatch circuit (see unit 18 in Fig. 1) configured to dispatch said instructions for execution by said plurality of execution units (see Dispatch Logic 74 and line that leads to execution units in Fig. 2);

a power management control unit (see unit 40 and 41 in Fig. 1, col. 5 lines 52 – 65, and col. 20 lines12 - 15) coupled to said instruction dispatch unit (see the signal lines SPS and HPS coming out from unit 40 and 41 in Fig. 1, and SPS and HPS lines leading to Dispatch Logic 74 in Fig. 2) , wherein said power management unit includes a programmable unit (see unit 40 in Fig. 1 and col. 5 line 59) for storing a particular value (col. 5 line 60) specifying a reduced power mode (col. 5 line 52);

wherein said instruction dispatch circuit (see unit 18 in Fig. 1) is configured to convey instructions (col. 20 line 5) to a restricted number (col. 20 line 8) of said plurality of execution units (see units 26, 22, 36, and 30 in Fig. 1) in response (col. 20 line 13) to said particular value (col. 5 line 60) being stored in said programmable unit (col. 20 line 12 – 13).

5. As per claim 2, Loper et al. teach a microprocessor as recited in Claim1 wherein said instruction dispatch circuit comprises an instruction alignment unit (see Sequencer Unit 18 in Fig. 1).

6. As per claim 4, Loper et al. teach the microprocessor as recited in Claim 1 wherein each of said plurality of execution units (col. 3 line 43) is included within a corresponding execution pipeline (col. 3 line 46).

7. As per claims 10, claim 10 is rejected based on the rejection of claim 1.

8. As per claim 11, Loper et al. teach the microprocessor as recited in claim 10 wherein said at least one execution unit (see Floating Point Unit 30 in Fig. 1) includes at least two execution units (see Fixed Point Unit 22 and Load/Store Unit 28 in Fig. 1) coupled (see the lines connecting them through the Sequencer Unit in Fig. 1) in a parallel, superscalar configuration.

9. As per claims 13 and 15, they are rejected based on the rejection of claims 2 and 4.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 3, 6 – 7, 12, 14, 16 – 18, 21 - 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loper et al., patent no. 5,805,907, and Kahle et al., patent no. 6,430,678.

12. As per claim 3, Loper et al. teach all of the microprocessor recited in claim 1.

Loper et al. do not teach a microprocessor wherein a plurality of execution units is configured to execute integer instructions.

Kahle et al. teach a microprocessor wherein an execution unit is configured to execute integer instructions (see Integer Unit 120 in Fig. 1).

It is the position of the examiner that a plurality of execution units configured to execute integer instructions is conventional, and it is also mentioned in Kahle et al.'s invention.

Therefore, it would have been obvious to include a plurality of execution units configured to execute integer instructions to Loper et al.'s microprocessor because such execution units are conventional.

13. As per claim 6, Kahle et al. teach the microprocessor further comprising a floating-point scheduler (see FIQ 213 in Fig. 2, and col. 4 lines 46 - 49) coupled to receive floating-point instructions dispatched from said instruction dispatcher (see Rename Mapping/ Dispatch in Fig. 2).

It is the position of the examiner that a floating-point scheduler is conventional, and it is also mentioned in Kahle et al.'s invention. Scheduling floating-point instructions

is a necessary functionality in pipelined microprocessors, and although it is not mentioned explicitly in Loper et al.'s invention, the fact that the invention contains a floating point unit (see 30 in Fig.1) and the fact that the invention is a pipelined system (col. 3 line 46) implicitly suggest that Loper et al.'s invention has some kind of functionality of scheduling floating-point instructions.

Therefore, it would have been obvious to include a floating-point scheduler to Loper et al.'s microprocessor because such a component is conventional.

14. As per claim 7, Kahle et al. teach the microprocessor as recited in Claim 6 further comprising at least one floating-point execution pipeline (see FPU0 212a and FPU1 212b in Fig.2) coupled to receive said floating-point instructions (col. 3 line 63) from said floating-point scheduler (see FIQ 213 in Fig. 2, and col. 4 lines 46 – 49).

15. As per claim 12, Loper et al. teach the microprocessor wherein said programmable unit includes a counter (col. 5 line 63 –64) containing a value (col. 5 line 60) that is modified upon the software event, wherein a particular value (col. 5 line 60) controls the stall of said selected instructions (see Abstract).

Loper et al. do not explicitly teach that the counter value is modified upon each dispatch cycle.

However, Loper et al. teach the counter value is modified upon the software event, which implicitly implies that its value can be modified at any dispatch cycle when the software event arises.

Therefore, it would have been obvious to see that Loper et al. teach a counter containing a value that is modified upon each dispatch cycle, wherein a particular value controls the stall of said selected instructions.

16. As per claims 14, 16 – 18, they are rejected based on the rejection of claims 3, 5 – 7.

17. As per claim 21, Loper et al. teach a microprocessor comprising:

a processor subunit (see unit 14 in Fig. 1) configured to perform a designated functionality (col. 3 lines 3 – 9) during each of a plurality of successive processing cycles; and

a power management control unit (see unit 40 and 41 in Fig. 1, col. 5 lines 52 – 65, and col. 20 lines12 – 15) coupled (see HPS and SPS lines connected to unit 14 in Fig. 1) to said processor sub-unit (see 14 in Fig. 1), wherein said power management control unit is configured to cause said processor sub-unit to *partially* stall (col. 8 lines

61 – 64) during selected processing cycles (col. 9 line 2) in response to said power management unit being programmed in a reduced power mode (col. 8 lines 57 – 58).

Loper et al. do not teach explicitly teach a power management unit configured to cause said processor sub-unit to completely stall during selected processing cycles.

However, Loper et al. teach a number of different levels to cause said processor sub-unit to partially stall (compare the number of amplifiers active between col. 8 lines 61 – 63 and col. 9 11 – 14). Loper et al.'s invention realized the stall of the sub-unit by inactivating some of the amplifiers in the instruction cache. Loper et al.'s invention revealed the method of inactivating some of the amplifiers, and by doing so, stalling the instruction cache. Therefore, it would have been obvious to one of ordinary skilled in the art to completely stall said processor sub-unit by inactivating all of the amplifiers.

18. As per claim 22, Loper et al. teach the microprocessor as recited in claim 21 wherein said processor sub-unit comprises a cache memory (see unit 14 in Fig. 1).

19. As per claim 23, Loper et al. teach the microprocessor as recited in claim 22, wherein said cache memory is an instruction cache coupled to provide instructions to at least one execution pipeline (see Fig. 1).

20. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Loper et al., patent no. 5,805,907, Kahle et al., patent no. 6,430,678, and Simar, Jr. et al., patent no. 6,182,203.

21. As per claim 5, Loper et al. in view of Kahle et al. teach all of claim 4.

Loper et al. in view of Kahle et al. do not teach the microprocessor wherein each corresponding execution pipeline includes a decode unit coupled to receive instructions from said instruction dispatch circuit and a reservation station coupled to receive a decoded instruction from said decoder.

Simar, Jr. et al. teach a microprocessor wherein each corresponding execution pipeline includes a decode unit coupled to receive instructions from a instruction dispatch circuit (see Fig. 24).

Kahle et al. teach a reservation station coupled to receive a decoded instruction from said decoder (see 204 coupled to 211 ~217 in Fig.2).

Loper et al.'s invention is motivated to provide a microprocessor that reduces power consumption and it provides a way to do so by restricting the number of instructions dispatched to the execution units when the microprocessor is in special mode.

However, it is well known in the art that significant power consumption in the pipeline occurs in the decoding stage (IEEE article 'Instruction Flow-Based Front-end Throttling for Power-Aware High-Performance Processors' by Amirali Baniasadi and Andreas Moshovos 6 –7 Aug. 2001, see third paragaph of the Introduction).

In Loper et al.'s invention, the instructions are decoded before they are dispatched. This means that Loper et al.'s invention loses significant power saving through the process of decoding before the it realizes the power saving by restricting the number of instructions dispatched.

Therefore, it would have been obvious to one of ordinary skill in the art to modify Loper et al.'s invention with Kahle et al.'s and Simar Jr. et al.'s inventions so that a decode unit would be coupled to receive instructions from instruction dispatch circuit and a reservation station coupled to receive a decoded instruction from said decoder.

Allowable Subject Matter

22. Claims 8 – 9, 19 – 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chi Whan Chung whose telephone number is (703)305-8788. The examiner can normally be reached on Monday~Friday 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703)305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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